

Multi-Carrier TD-SCDMA Feasibility

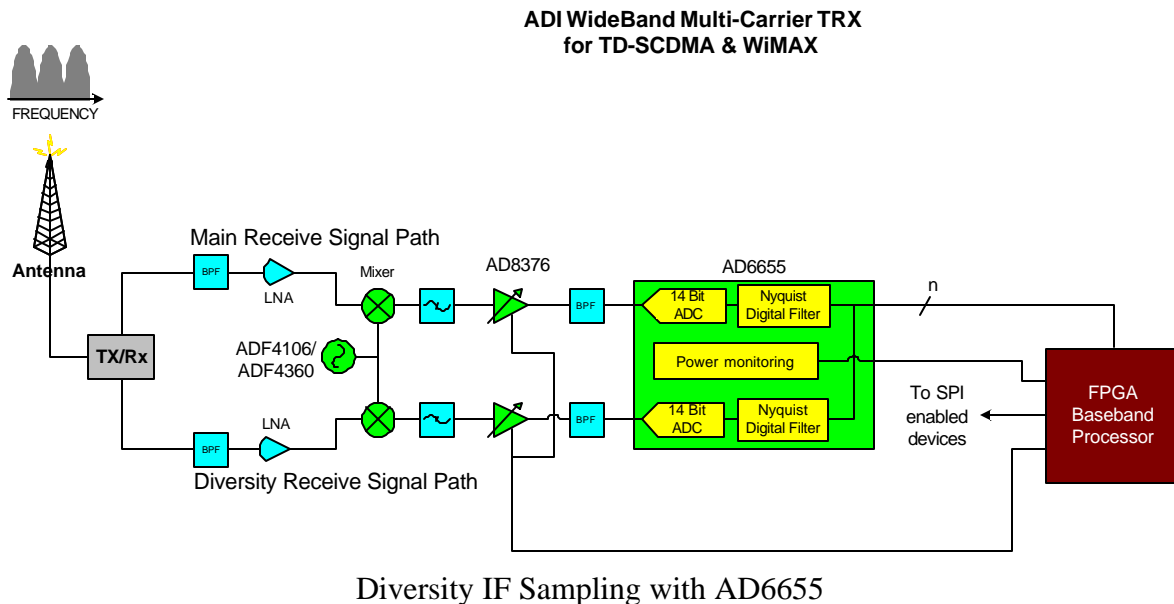
Brad Brannon, Analog Devices, Inc.

Abstract

The goal of this discussion is to determine the feasibility of implementing a multi-carrier 3G transceiver and what the major subsystem performances must be.

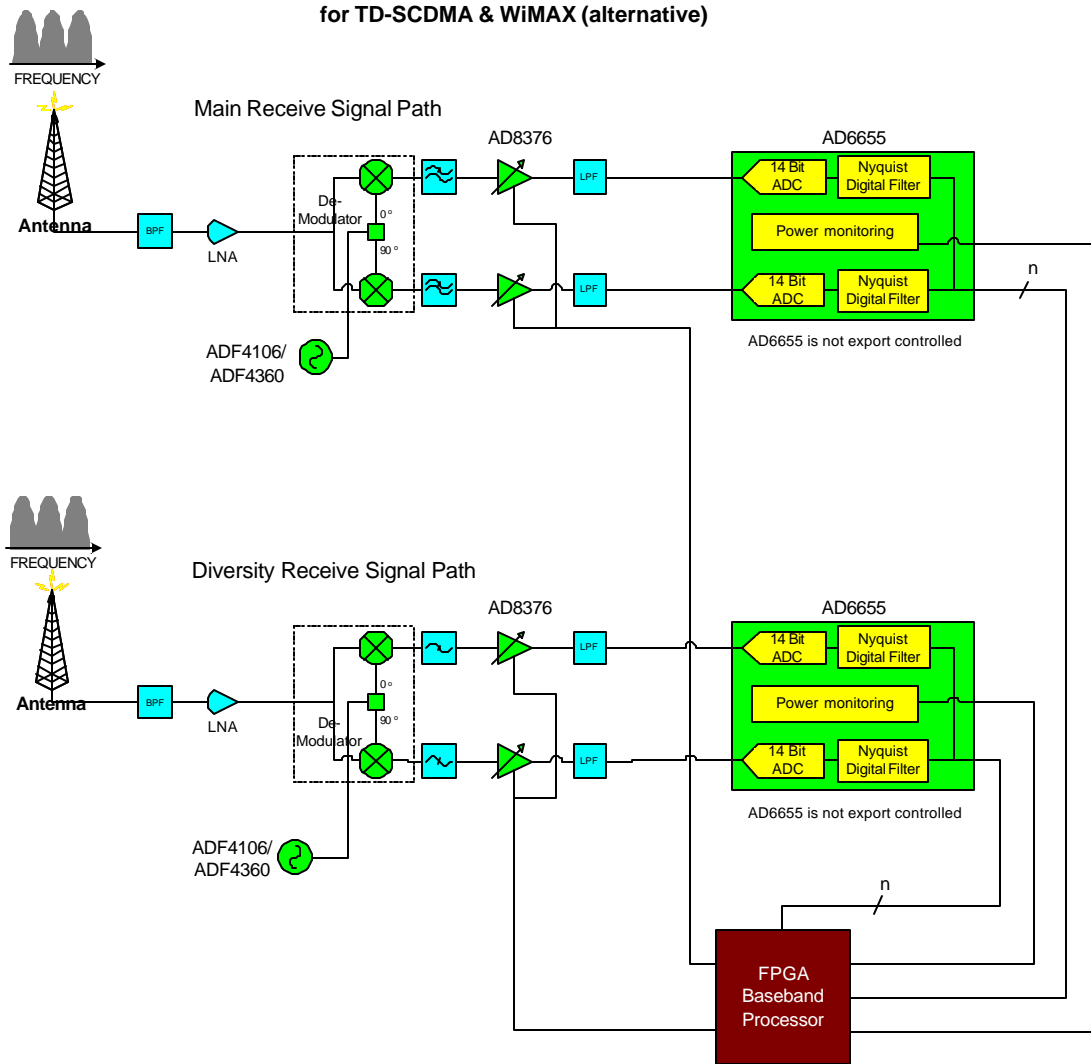
General Architecture

The block diagram shown below is the general block diagram used in this discussion. While there are many variations of this design, the key focus will be on this architecture. This architecture represents a flexible radio platform that can easily be used to implement a wide variety of air standards including TD-SCDMA, WCDMA, CDMA2000 and WiMAX.



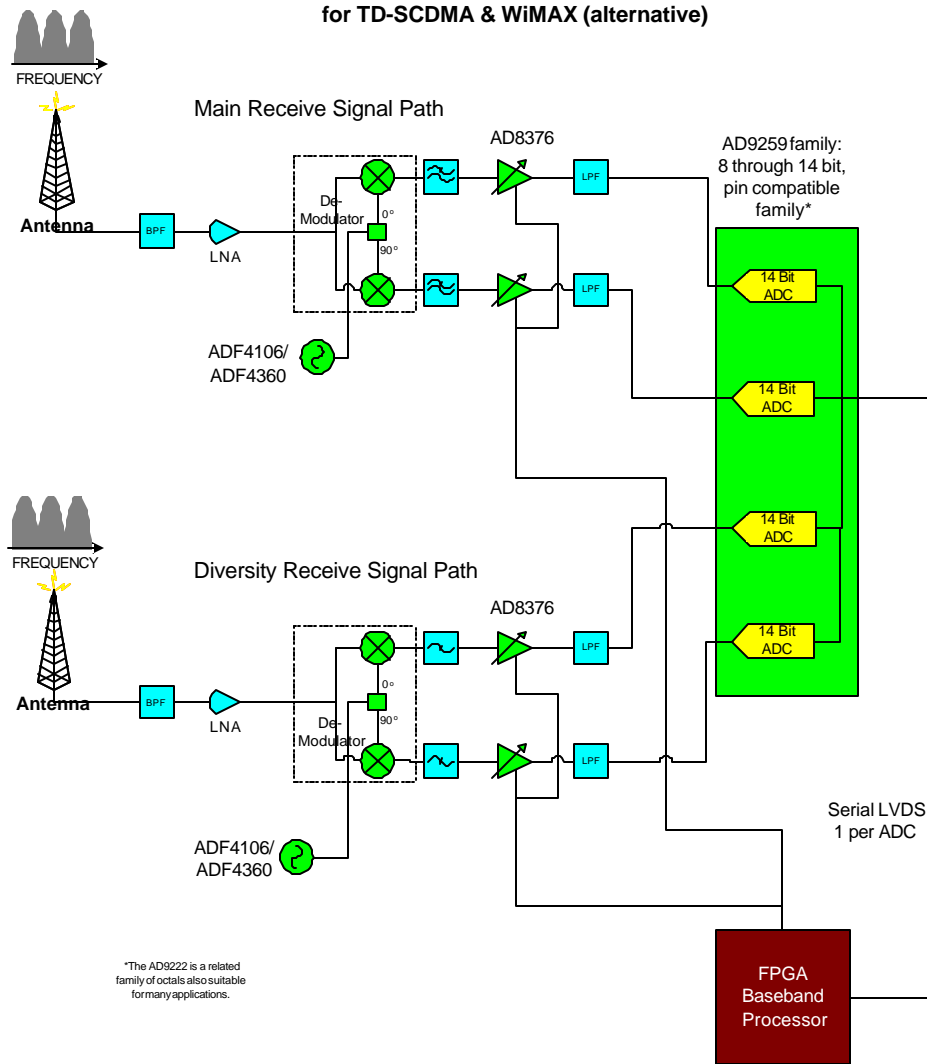
This diagram is suitable for both low and high IF sampling as the AD6655 is suitable for either. In addition to the ADCs for sampling, the AD6655 includes digital tuning, decimation and fixed filtering to provide 20 MHz of spectrum with >100 dB stop band rejection. Other key features include low latency peak power detection and rms signal measurement capabilities, both of which are useful for accurate AGC control. In addition, the AD6655 is suitable for direct conversion. Although direct conversion is difficult for multi-carrier TD-SCDMA, WCDMA and CDMA2000, it is quite suitable for WiMAX applications given that no sub-carriers are placed at DC. Other architectures are also possible. These include baseband sampling using quad and octal ADCs such as the AD9228 & AD9259 and AD9222 & AD9252. These products allow package to digitize 2 and 4 carriers respectively (1 or 2 main and diversity paths respectively). One final option is to use the AD6654 which includes an IF sampling ADC and 6 channel DDC.

**ADI WideBand Multi-Carrier TRX
for TD-SCDMA & WiMAX (alternative)**



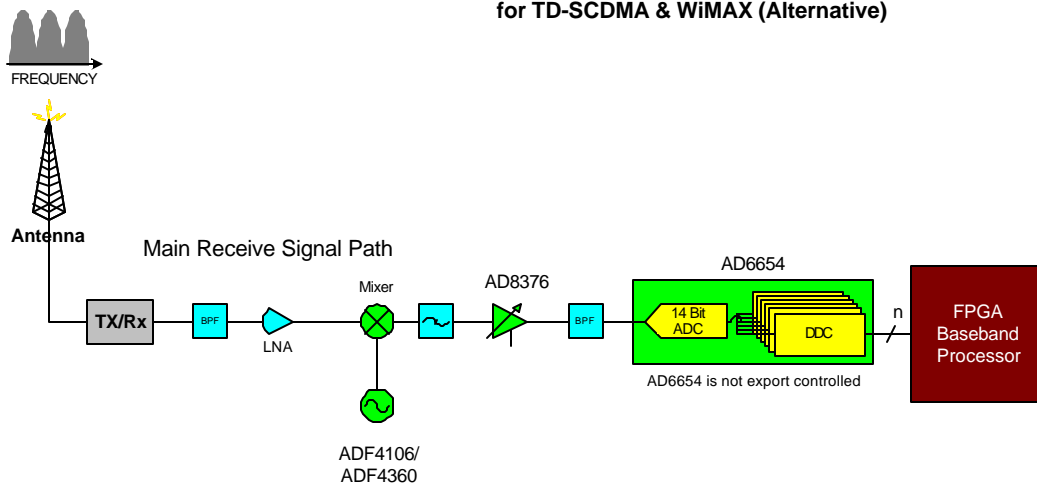
Diversity Baseband Sampling with the AD6655

**ADI WideBand Multi-Carrier TRX
for TD-SCDMA & WiMAX (alternative)**



Diversity Baseband sampling with the AD9259 (AD9228)
(The AD9222 or AD9252 will allow 2 carrier diversity baseband sampling with one ADC)

ADI WideBand Multi-Carrier TRX for TD-SCDMA & WiMAX (Alternative)



IF sampling using the AD6654 (2 required for diversity)

Each of these solutions provides high levels of integration. Some solutions provide integration of multiple ADCs. Some provide integration of ADC and digital content. Others provide integration of ADC and analog content. Still others, such as the AD6655, provide integration of both analog and digital content on the same chip. It is with that in mind that the following discussion is offered. While the general discussion applies to the other configurations, only the AD6655 offers a compact, well rounded integration solution. The other integration solutions may offer other benefits depending on the architectures.

TD-SCDMA Requirements

Specifications for this report are taken from the requirements for Wide Area BS as defined by 3GPP TS 25.105 V7.1.0, specifically section 7. Key specifications from this standard are the reference sensitivities, band of deployment and blocking requirements. It is assumed that the Node B terminal will not be required to meet the sensitivity and blocking requirements of different platforms at the same time. Meeting the sensitivity of a wide area BS while also matching the blocking requirements of the local area BS may be desirable, but is not the goal discussed here. It should be noted that the requirements of a Node B terminals for medium and local area BS have similar dynamic range requirements to the wide area version with the exception that the level planning is shifted up to account for the larger expected signal levels. These can be accommodated within the same design by shifting the level plans upward as these systems can also tolerate increased noise.

Receiver Operating Conditions

From the standard, the required minimum reference sensitivity is -110 dBm within a 1.28 MHz channel bandwidth. On a per Hertz basis, this is a signal density of -171.1 dBm/Hz. Where noted, the WCDMA test conditions specify -104 dBm/1.28 MHz (-165.1 dBm/Hz) also applies.

The second set of conditions is the adjacent channel selectivity. For a 1.28 MHz channel, the desired channel is -104 dBm and the interfering signal is -55 dBm representing a single code CDMA carrier.

The third set of conditions is the blocking requirements. For a 1.28 MHz channel in the specified deployment band, the desired channel is -104 dBm and the blocker shall be -40 dBm at 3.2 MHz offset represented by a narrow band CDMA signal. For signals outside of the deployment band, the blocking tolerance should be -15

dBm represented by a CW carrier. When co-located with GSM, the requirement is +16 dBm and when co-located with a UTRA-FDD, the requirement is +13 dBm represented by a CW tone in both cases.

The final set is that of intermodulation. The CW case is more restrictive and therefore, 2 CW tones of -48 dBm are required to in the presence of a signal at -104 dBm. These tones have a 3.2 MHz offset.

Assumptions

The primary focus of this document is ADC requirements. Therefore, co-location issues must largely be handled in the RF and IF portions of the receiver using aggressive analog filtering techniques. Even still, it is anticipated that some amount of co-location signal will pass the RF and IF signals, especially in the adjacent allocation cases, resulting in signals only attenuated by as little as 30 to 40 dB. It will be assumed that nearby co-location spurious can be reduced to -40 dBm, a reduction of about 56 dB for the GSM case, thereby matching the blocker requirements assumed here. Depending on the deployment band for the receiver, the co-location requirement may be at the immediate band edge. With that in mind, analog filtering may not totally remove the signal from the spectrum passed to the ADC. Therefore the ADC must provide adequate oversampling that the Nyquist filter removes the remainder of the co-location signal before it aliases back into the useful processing spectrum of the ADC. Best case, if the RF and IF filtering reduces the input referred co-location blocker to -40 dBm (56 dB attenuation), this will match the in-band blocker requirements and take only 3 dB of additional head room.

The second assumption is that the fullscale of the ADC is 2 volts peak to peak into a 200 ohms termination. This requires an rms drive level of +4 dBm for a sinewave or a peak drive of +7 dBm.

If it is assumed that the largest in band signal is -40 dBm, the minimum conversion gain may be calculated. If the fullscale of the ADC is +4 dBm and the largest inband signal is -40 dBm with an assumed 10 dB peak to average ratio, a gain of 34 dB would be sufficient. Ideally 3 additional dB of margin should be allocated for unfiltered co-location blockers reducing the gain potentially to 31 dB. This will be reviewed below. A higher gain could be allowed in non-blocking environments if desired but is not strictly necessary to meet the requirements. Products such as the AD6655 include advanced features that greatly simplify the AGC function required to support these operations. Given current receiver trends in LNAs, passive mixers and filter elements, typical down-converters blocks with this gain are possible with a noise figure of 3 dB, not including the ADC. These numbers will be used in the following calculations.

Converter sample rates up to 122.88 MSPS are viable. 1.28 and 3.84 are both factors of this number and both yield rich factors of two making this a nice sample rate when integer decimation is used in the digital domain to implement channel filtering. Other sample rates are also possible include 92.16 and 76.8, both of which include many powers of two for decimation purposes.

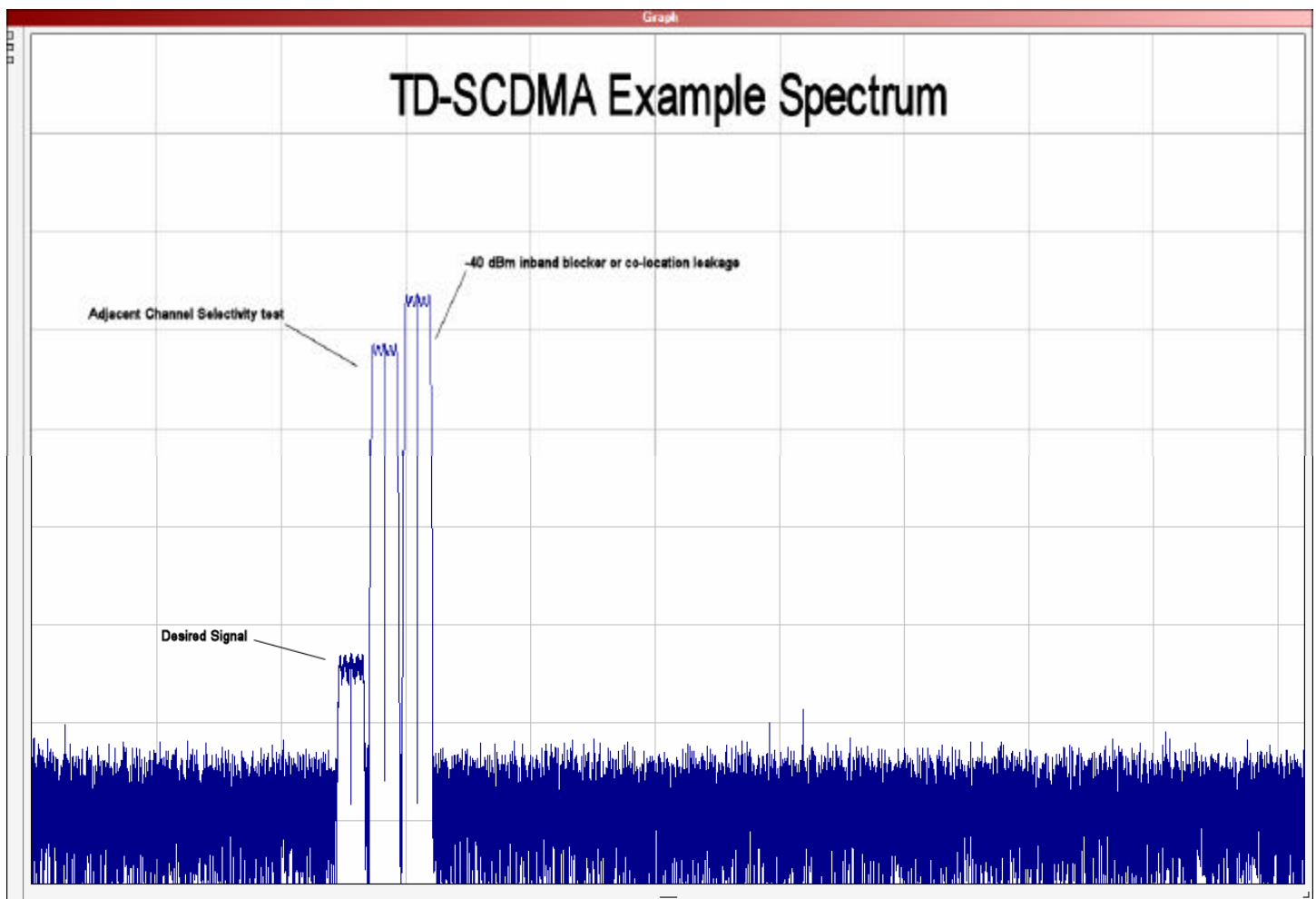
ADC SNR Requirements

Given the conversion gain and NF above, the ADC SNR can now be calculated. At the antenna, the noise spectral density is assumed to be -171.1 dBm/Hz. Given the conversion gain and noise figure previously stated, the noise spectral density (NSD) at the ADC input will be -137 dBm/Hz (-174 plus 34 plus 3). This assumes that noise outside the Nyquist band of the ADC will be filtered using anti-aliasing filters to prevent front end thermal noise from aliasing when sampled by the ADC. If the ADC noise floor is 10 dB below that of the front end noise, it will contribute about 0.1 dB to the overall NF of the receiver. Therefore, a maximum ADC noise floor of -147 dBm/Hz should be allowed. Higher ADC noise floors can be used but as the ADC noise begins to contribute to the floor of the receiver, some of the non-linearities described in "DNL and Some of its Effects on

Converter Performance” found in Wireless Design & Development Online June 2001 online issue may adversely impact receiver performance, especially when it comes to signal power estimation. Therefore, the ADC noise floor should be as small as reasonable without over-designing.

For IF sampling, the total noise in the Nyquist band of the ADC can be determined by simple integration. Over 61.44 MHz (the Nyquist band of 122.88 MHz) the total noise is found to be -69.2 dBm. If the rms fullscale of the ADC is +4 dBm, this is a required minimum fullscale SNR of 73.2 dB. If gain is reduced by the additional 3 dB for co-location feed through, this would require an SNR of about 76 dB. In the absence of blockers, the conversion gain could be increased, reducing the required performance of the ADC. Similarly, the gain could be slightly reduced (by about 3 dB using this gain plan) if a signal greater than -40 dBm (relative to the input) is present. As noted before, the AD6655 can be assigned this task using the Fast Detect output bits. In summary, a minimum SNR of about 73 dB should be allocated to the ADC. Slightly less could be tolerated but will sacrifice performance in terms of both spurious and closed loop power control.

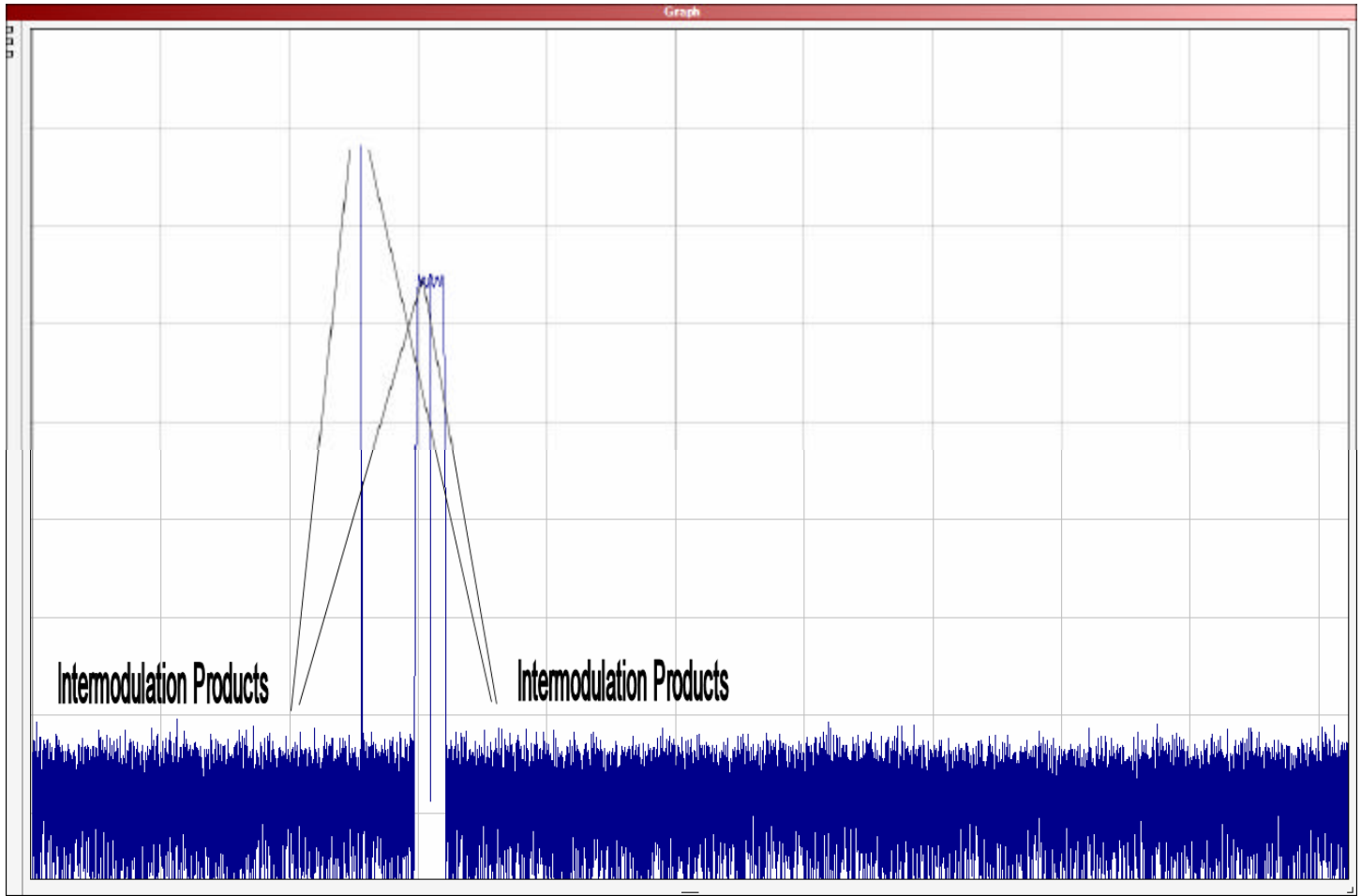
Adjacent channel selectivity should not be an issue under these circumstances. With a gain of 34 dB and an adjacent channel of -55 dBm, the resulting adjacent channel would be -21 dBm as presented to the ADC and the resulting desired signal would be -70 dBm. Under these conditions, the channelization filter would need to provide about 65 dB of rejection. It is not difficult to get 100 dB of rejection. Further offset from the desired carrier, the signal level is -40 dBm analyzed above and would require about 80 dB rejection by the channelization filter.



TD-SCDMA waveform with Adjacent Channel and In-band blockers

ADC SFDR Requirements

Spurious performance is a little less obvious from the specifications. However, there are several guidelines in the standard that provide SFDR requirements. These are primarily found in the single and two tone blocking specification. No matter the source of the spurious, the resulting tone should not disrupt receiver sensitivity. In all test cases where blocking or interferers are present, the desired signal is 6 dB above reference sensitivity. If the energy from the spurious is allowed to equal the noise floor, overall sensitivity will be reduced by 3 dB, however, the signal is allowed to increase by 6 dB, leaving an extra margin of 3 dB.



TD-SCDMA Intermodulation Products

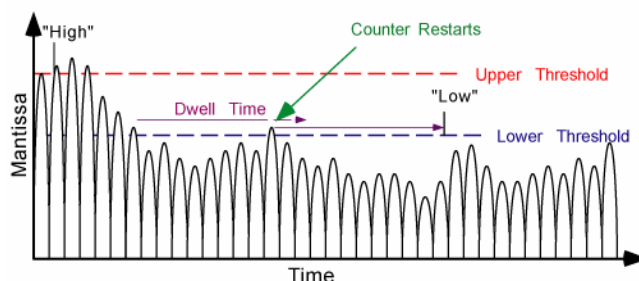
To minimize impact of the spurious products, they should contribute no more than the thermal noise floor should. Thermal noise in 1.28 MHz at the antenna is -113 dBm/1.28 MHz. Including conversion gain and NF, this is -76 dBm/1.28 MHz at the ADC input. Therefore, the intermodulation and spurious products of the ADC should be no larger than -76 dBm or -80 dBFS reflected back to the ADC input. Because this is total spurious energy, it must be shared between the ADC and analog front end. Therefore, an addition 3 or more dB need to be allocated to the ADC bringing the total spurious performance of the ADC to -83 dBFS. This is the spurious performance required, regardless of the sources (SFDR, IMD and other).

	SNR	Spurious (SFDR, IMD and other)
Minimum ADC Performance	73 dBFS min	83 dBFS min

ADC minimum required performance to prevent ADC non-linearities from disrupting performance.

Comments on Gain, fixed or variable

The case presented here indicates that fixed gain is possible for a TD-SCDMA implementation. Even if gain control is not needed, it may be desirable to implement protection from input clipping. Regardless of the need, the AD6655 can aid in both gain control and clip prevention by utilizing the fast detect bits of the converter. The fast detect bits function similarly to an overflow bit on a converter. The key difference is that they may be programmed to detect signals that peak between 0 and -30 dBFS in a logarithmic fashion. The latency on this function is only 2 clock cycles, reducing the delay and allowing fast response during signal peaking. The chip also includes a lower threshold detection and dwell time setting that detect when the envelop falls below a programmable level allowing the gain to be increased after clipping. The latency on the lower threshold is longer and used in conjunction with the dwell time associated with the built in hysteresis used to prevent re-modulation of the signal. In addition to the various level detectors that may be used for gain control, the chip includes a full featured power measurement circuitry. This circuit can be used to measure the power of either a main and diversity signal as well as the power of an I & Q signal. The power can be read through the SPI registers or through a dedicated high speed serial data interface making it a useful addition to applications that require tight power control of detected signals and full featured automatic gain control and power measurement systems.



AD6655 Gain Control features

Validation

Given a gain of 34 dB an analog front end NF of 3 dB, what levels of performance can be expected? Additionally, what improvements can be made if gain is increased and decreased by 6 dB? The table below shows how residual SNR and ADC clip point will change as a function system gain. It should be noted that spurious that fall inband and have energy equal to the noise floor (-83 dBFS) will degrade performance by 3 dB. Sufficient margin exists to tolerate about 6 dB degradation from combined ADC and analog front end distortion plus noise generated from clock jitter and system phase noise. Refer to AN-501 and AN-756 for more information on system phase noise and clock jitter.

Gain	AFE NF	0 dB SNR (after despread)	Effective SNR @ -110 dBm*	ADC clip point (CW tone)
28 dB	6 dB	-125.9 dBm	-4.1	-24 dBm
34 dB	3 dB	-129.8 dBm	-0.2	-30 dBm
40 dB	3 dB	-129.9 dBm	-0.1	-36 dBm

*not including despreading factor. Note also that for most blocking tests this number is increased by 6 dB.

Margin for a 6 carrier receiver

The assumption for this entire discussion has been that this is a wideband receiver and the requirements in SNR and SFDR have been derived with that in mind. It is possible to trade off performance in these regards by adding analog channel filtering (SAW filters) but the specification here assume no narrowband filtering.

With 6 carriers in band, each signal must be backed off between 17 and 20 dB to account for equal accumulated power plus combined peaking. With 34 dB of gain, the rms clip point is -30 dBm. Allowing 7.8 dB for 6 carriers and 12 dB for peaking, the maximum single tone power should be -49.8 dBm. If one of the carriers is set to -110 dBm, without the influence of the other 5 carriers, the SNR before despreading can be determined from the chart above to be about 0 dB (-0.2). After de-spreading this should be about 20 dB. In multi-carrier applications, the desired sensitivity should require -104 dBm sensitivity in which case, the SNR would be 6 dB higher or 26 dB. Only about 5 dB is required. The net effect is that intermodulation can degrade performance by 21 dB before performance becomes an issue.

Revisions:

A – June 29, 2006 Initial Draft

B – July 6, 2006 with feedback from JH

C – July 6, 2006 to align with PowerPoint

D – Remove footer

E – March 12, 2007 Update Part Numbers